ABSTRACT OF THE DISCLOSURE

An example computer system includes a first bridge device that includes an interface controller. The interface controller combines debug information generated within the bridge device with a training pattern. The first bridge device is coupled to a second bridge device via a high-speed asynchronous interconnect. The first bridge device converts the debug information and training pattern into a packet to be transmitted over the interconnect to the second bridge device. The training pattern serves to allow the second bridge device to maintain bit and symbol synchronization during the transfer of the debug information.